WHAT IS CLAIMED IS:

1. A method for manufacturing a package substrate without using any plating lead line, comprising the steps of:

a) plating copper on all surfaces of a base substrate formed with a plurality of through holes and inner surfaces of the through holes, thereby forming a first copper plated layer;

b) coating a first resist for a plating process over the first copper plated layer, partially removing the first resist, thereby exposing predetermined portions of the first copper plated layer respectively corresponding to regions where circuit patterns are to be plated;

c) plating copper on the exposed portions of the first copper plated layer, thereby forming a second copper plated layer;

d) stripping the first resist remaining on the first copper plated layer;

e) coating a second resist for a plating process over all surfaces of a structure obtained after completion of the step (d), and removing the second resist from regions where wire bonding pads and solder ball pads are to be formed;

f) removing portions of the first copper plated layer exposed without being covered by the second resist, by use of an etchant;

g) forming an Au layer on portions of the second copper

plated layer exposed without being covered by the second resist in accordance with an electrolytic Ni-Au plating process, thereby forming the wire bonding pads and the solder ball pads;

h) removing the second resist remaining on the structure by use of a stripping solution;

i) removing portions of the first copper plated layer exposed in accordance with the removal of the second resist, by use of an etchant; and

j) coating a solder resist over all surfaces of a structure obtained after completion of the step (i), and removing portions of the solder resist respectively covering the wire bonding pads and the solder ball pads.

2. The method according to claim 1, wherein the first copper plated layer is formed in accordance with an electroless copper plating process.

3. The method according to claim 1, wherein the second copper plated layer is an electrolytic copper plated layer, and forms the circuit patterns.

4. The method according to claim 1, wherein the second resist is a dry film for an Au plating process.

5. The method according to claim 1, wherein the Au layer

plated in accordance with the electrolytic Au-Ni plating process has a thickness of 0.5 to 1.5μm.

6. The method according to claim 1, wherein the first copper plated layer serves as a plating lead line during the electrolytic Au-Ni plating process for the wire bonding pads and the solder ball pads.

7. A package substrate electrolytically plated with Au without using any plating lead line, comprising:

a base substrate formed with a plurality of through holes;

a first copper plated layer plated on predetermined portions of the base substrate and inner surfaces of the through holes;

a plated pattern layer formed on the first copper plated layer;

wire bonding pads formed on predetermined portions of the plated pattern layer at an upper surface of the base substrate in accordance with an electrolytic Au plating process without using any plating lead line;

solder ball pads formed on predetermined portions of the plated pattern layer at a lower surface of the base substrate in accordance with an electrolytic Au plating process without using any plating lead line; and

a solder resist covering the base substrate and the plated pattern layer, except for the wire bonding pads and the solder ball pads,

the plated pattern layer being formed by coating a resist on the first copper plated layer, except for regions around the through holes, and forming a second copper plated layer in a semi-additive manner on portions of the first copper plated layer at which the resist is not present.

8. The package substrate according to claim 7, wherein the wire bonding pads and the solder ball pads are Au layers plated in accordance with application of current to the first copper plated layer.

9. The package substrate according to claim 7, wherein the first copper plated layer serves as a plating lead line during the electrolytic Au plating processes for the solder ball pads and the wire bonding pads.

10. The package substrate according to claim 7, wherein each of the electrolytic Au plating process forms a plated layer having a thickness of 0.5 to 1.5μm.

11. The package substrate according to claim 7, wherein the first copper plated layer is an electroless copper plated

layer.